



Design Note 002

Design For Packageability

Rick Sturdivant,
rsturdivant@mptcorp.com

For highest performance and lowest cost, ICs and modules must be designed for integration into packaging. Often, the IC design is complete and fabricated before any serious consideration is given to packaging issues. However, it is often too late to take advantage of IC design changes that can improve packaged performance. This can result in degraded performance at the package level. Furthermore, at the package level it is often discovered that simple passives such as capacitors, inductors or resistors are required. If the package design is conducted in parallel with the IC, very often passives can be integrated into the IC, which improves package level performance. This can result in lower cost since it can be cost effective to integrate some passives at the IC level thereby eliminating the cost of placing and wire bonding passives. This is especially true for high speed and millimeter-wave ICs and modules.

Introduction: For many ICs and modules, the path to lowest cost and smallest size is to perform IC design and package design in parallel. Often, the IC is designed and fabricated before any serious consideration is given to packaging issues. At that point, it is often too late to take advantage of IC design changes that can improve package level performance and reduce size. This can result in degraded performance at the package level, larger size and increased cost.

Furthermore, at the package level it is often discovered that simple passives such as capacitors, inductors or resistors are required. If the package design is conducted in parallel with the IC, very often passives can be integrated into the IC that improve package level performance. This can result in lower cost since it can be cost effective to integrate some passives at the IC level thereby eliminating the cost of placing and wire bonding passives. This is especially true for high speed and millimeter-wave ICs where the relative value of the required passives is low and the resulting elements are easily integrated into the IC. Very often, it is not possible

to integrate passives into the package or chip caps are used. This is especially true for very small single IC packages in ceramics such LTCC, HTCC or in liquid crystal polymer (LCP) packages.

Goal: Optimum Total Performance

Total performance is the performance of the package and the IC integrated together. This is illustrated in Figure 1. Note how the total performance is equal to the IC plus the package. While this is a simple and on the surface very obvious fact, many designers and product developers tend to forget or ignore this during design.

$$\text{Total Performance} = \text{IC} + \text{Package}$$
The equation is visually represented with two small images. The first image is a square integrated circuit (IC) chip with a complex pattern of gold wire bonds. The second image is a square package, likely a ceramic or LCP package, with a yellowish surface and some internal components visible.

Figure 1. Total performance is equal to the IC performance plus the package performance.

Packaging Considerations

There are several considerations to keep in mind when developing packaging in parallel with IC design. Several of these are briefly considered and key elements are discussed.

Isolation and Coupling. Isolation is an issue and a concern for packages which have high gain, high speed/high frequency, long wire bonds, adjacent signals or power, inductive paths to ground or very low signal levels adjacent to very high signal levels.

An example where isolation is a concern is in a single IC high-speed package that has 35dB gain operating at 10Gb/S or more. This is a concern, since coupling generally increases as frequency increases. If signal from the output leaks back to the input it can cause oscillations. Often the placement of the IC I/O can be configured to minimize coupling. Also, grounding pads can be added on the IC and connected to the package to aid in isolation.

Resonances. Undesired resonances can occur at the package level, in bias circuits, in the ground plane, or in the circuits connected to the IC. Resonance and oscillations are different. A resonance does not necessarily lead to instability and oscillation. For instance, a resonance can cause an insertion loss pole in the desired pass band. These effects often cannot be determined at the IC level, but the IC design can minimize these effects.

Biasing: Most electrical circuits require some type of electric bias to function. Injecting this bias into the circuit requires proper design of the bias circuit on the IC and package. By proper design, many of the circuits can be moved off the IC package and into the IC.

Ground Loops: Some ICs require separate ground paths for digital and rf sections. Other ICs require different grounding for channels in the IC. An incorrect ground path can cause issues with common mode

ground path inductance in differential circuits. However, the I/O on the IC and bypass capacitors can often be used to minimize this effect.

Wire Bonds: The presence of wire bonds in high speed and millimeter-wave circuits can affect electrical performance significantly. Proper design of the IC can minimize this effect. For instance, simple capacitive matching can be placed on the IC. Figure 2 shows a 3D model in HFSS of a wire bond. This model was used by MPT to develop a parameterized model of the wire bond. Proper design of the IC taking into account packaging and wire bonds can be very important for high speed products.

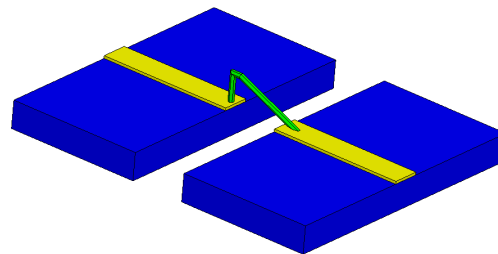


Figure 2. 3D model in High Frequency Structure Simulator (HFSS) of a wire bond.

Thermal Path: The thermal path out of the IC is very often not considered until the IC design is complete. However, proper IC design of gain distribution, placement of heat generating devices and bias design can improve packaged performance.

Conclusions

Proper design of the packaging in IC and module designs can have a significant effect on the cost and size of the resulting packaged product. Instead of designing the packaging after the IC is designed, the packaging and IC should be designed in parallel.