The Evolution of Packages for Monolithic Microwave and Millimeter-Wave Circuits

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Abstract—The maturing of monolithic microwave integrated circuit (MMIC) technology has spawned a variety of new military and commercial applications. As a result, there is an increased emphasis on the packaging of MMIC chips and MMIC-based components. Currently, the industry is applying a number of new assembly and packaging technologies to RF components and subsystems driven by the forces of performance, size and weight, and cost. This paper outlines the current evolution in microwave and millimeter-wave packaging using examples drawn from the area of active array antennas.

I. INTRODUCTION

THE maturing of monolithic microwave integrated circuit (MMIC) technology together with rapidly emerging commercial markets in areas such as telecommunications and automotive has spawned a variety of new military and commercial applications at microwave and millimeter-wave frequencies.

As a result, there is an increased emphasis on the packaging of MMIC chips and MMIC-based components. Concurrently, a number of new assembly and packaging technologies are being applied to RF components and subsystems. At the application or product level, MMIC packaging is driven by the forces of performance, size and weight, and cost. At the same time, the technology is moving toward increasing functional complexity, and consequently, multichip packages and modules.

In this paper, we will outline the current evolution in microwave and millimeter-wave packaging through a series of examples of newly emerging technologies and applications. Since much of the recent RF packaging development activity is being driven by the potential of very large numbers of transmit/receive (T/R) modules required for future Department of Defense ground, airborne, and space-based active array antennas, much of the work described in this paper is related to these modules.

II. PACKAGE FUNCTIONS

All electronic packages must provide a series of interrelated electrical, mechanical, and thermal functions which impact the performance of the device(s) contained within them. Electrically, the package must provide a means of conveying electrical signals between the external environment and the internal operating environment of the package. This function must be implemented with controlled impedance levels and minimal interference between signal paths. Thermally, the package must provide heat sinking for internal active devices to maintain low operating temperature for maximum life. Mechanically, the package must be physically strong, provide protection for its internal elements from hostile environments, and be manufacturable at reasonable costs.

In providing these functions, the package always degrades the RF performance of the electronic components which it contains. Reduced performance may take the form of lower output power, increased noise figure, or narrower bandwidth. The amount of performance degradation increases with operating frequency and reduced dimensional tolerances.

A. Electrical Interface

The electronic package must provide means for coupling dc, RF, and in some cases control or logic signals into and out of itself. This should be accomplished with, ideally, no degradation in the performance of the electronic components contained within the package. This, of course, is never realized in practice as discussed below. Coming as close as possible to achieving this goal, however, must remain a primary goal of the package designer. To meet this objective, careful attention must be given to package design and simulation, choice of materials and assembly processes, as well as the variability associated with the manufacturing process, areas which have received insufficient attention to the present.

B. Thermal Interface

The demand for ever-increasing power from millimeter-wave and microwave devices has spurred improved thermal design for packages. Table I lists some common substrate materials along with their respective thermal conductivities [1], [2]. Typical package designs in the past have used a substrate attached to a metal package similar to the receive-only module shown in Fig. 1. This design approach increased the thermal resistance and resulted in a possible mismatch between the coefficient of thermal expansion (CTE) of the GaAs chips, the substrate material, and the package material. A better design is to use the substrate as part of the package, thus reducing the thermal path. Typically, the peak operating temperature of the chip should be kept below 120 degrees C to provide a lifetime that is consistent with the expected product life of 5–10 years [3]. The maximum temperature will vary with the activation
energy of the device. The chip temperature is dependent on the overall thermal resistance from the chip to the heat sink and the amount of heat generated on the device. The heat generated depends on the efficiency and average duty cycle of the device and its operating microwave power level. Microwave devices at 10 GHz are currently approaching efficiencies of 50% or more. Fig. 2 shows the thermal gradients of a 4-watt X-band microwave MMIC flip chip mounted on aluminum nitride. The efficiency of the chip is about 20%, and the duty cycle is 50%. Note that the major thermal gradients are between the chip and substrate and at the interface between the substrate and the heat sink. The package itself contributes only a minor percentage to the thermal resistance. For this particular design, the heat transfer is provided by thermal bumps that are attached to the sources of the FET’s.

C. Mechanical and Environmental Protection

The packaging of microwave circuits must provide protection against mechanical shock and vibration, thermal shock and cycling, and moisture and corrosion. At the beginning of the design cycle, it is important to specify the operating environment of the package. This environment will influence the choice of materials, attachment technologies, connectors, heat sinking, and cost. A formal trade-off analysis is performed to determine the packaging parameters that best meet the environmental requirements at the lowest possible costs. After performing the trade-off analysis, modeling of the packaging materials and attachment technologies is performed to predict the environmental performance of the package. The thermal stress generated in the package material can be predicted by CAD programs such as PATRAN and NASTRAN [4].

The reliability of the attachment technology can be predicted using empirical and experimental data to assess the fatigue lifetime under temperature cycling. During the layout of the microwave chips, a first-order approximation of the thermal profile of the chips and the substrate can be used to optimize chip locations and determine if thermal vias or other materials are necessary to reduce the thermal resistance. The design tools are becoming more refined and accurate and allow progressively more accurate simulation of the environmental performance. These tools have substantially reduced the number of design iterations.

D. The Influence of the Package on Performance

An electronic package, in general, will always degrade the RF electrical performance of the components (monolithic chips and hybrid assemblies) that it contains. The performance degradation stems from a number of fundamental physical effects which include:

1) Input and output port reflection and insertion losses:
   These losses are related to the inability to precisely control impedance levels at the package terminals as well as the resistive losses associated with transitioning the RF signal through the package walls.

2) Insertion and reflection losses associated with the interior of the package: These include losses associated with transmission lines within the package as well as reflection and insertion losses resulting from interconnecting active chips and other components within the package. Depending on the methods of assembly, the variability of these latter losses may be significant, for example, with chip and wire assembly. These effects increase with increasing frequency. For example, reactance variability resulting from chip and wire assembly which is
marginal acceptance acceptable at millimeter-wave frequencies.

3) Package-generated resonances and related effects: These may be excited by active circuit elements within the package and may be present within or outside of the operating bandwidth. In addition, package shielding effects, due to both higher order waveguide mode propagation and the close proximity of enclosure walls, can seriously perturb microstrip propagation and the effects of discontinuities within the package [5]. Many microwave engineers have had the experience of tuning an amplifier or other component for optimum performance, and after installing the package lid, see the component performance seriously degraded. While a goal of the package designer is certainly to address such problems early in the design cycle, it is evident that current tools are probably not yet capable of doing so.

III. CURRENT FORCES SHAPING MICROWAVE AND MILLIMETER-WAVE PACKAGE DEVELOPMENT

A. Economics

Both military and commercial users are driving down the cost of microwave packaging by developing technologies that provide high yielding batch processing of the package and substrate material. The costs associated with packaging are the package and substrate material and fabrication, assembly of the electronics into the package, and scrap and rework. The substrate materials are being driven to lower costs by batch processing. As an example, large area formats are being developed for processing polyimide and aluminum nitride substrates. Alumina substrates are already fired in large area formats (24" x 24"). The substrates are also designed to carry the microwave signals underneath the metal package rim by using coplanar or microstrip lines thus eliminating expensive microwave connectors.

The MMIC package requirements for the DoD are summarized below [6]:

- The military is developing net shape packages that require no additional machining after fabrication. ASIC is being cast in net shape packages by Ceramics Process Systems. Martin Marietta is developing electroformed packages for millimeter waves. Commercial houses such as Motorola are developing low cost plastic packages.
- To reduce the design, manufacturing, and test costs associated with packaging, the government is sponsoring the development of package design, modeling, and simulation tools. Presently, there are commercial software packages that have not been linked together to provide a seamless transfer of data for mechanical, thermal, and RF performance of the package. Some of these linkages will be performed on the ARPA and Tri-Service sponsored High Density Microwave Packaging Program (HDMPP). One of the major thrusts of this and future programs is the development of the databases for materials, devices, and interconnects, that will allow the designer to simulate the package performance with the integrated CAD tools. The success of this program will substantially reduce the package development cycle time and cost.

B. High Performance and Less Costly MMIC Chips of Greater Complexity

Stimulated by significant government investment through technology programs over the past 15 or more years and more recently through the MIMIC program, MMIC's have matured and are being applied to an increasingly broad range of military and commercial applications. These advances are based on and characterized by:

1) Maturing process and device technologies, the latter including, in addition to metal semiconductor field effect transistors (MESFET's), high electron mobility transistors (HEMT's) and heterojunction bipolar transistors (HBT's) employing both GaAs [7], [8] and InP [9], [10], substrate materials.
2) More sophisticated and increasingly accurate MMIC computer-aided design (CAD) tools and models which result in more “first pass” design successes.
3) MMIC circuits employing increasing numbers of transistors (currently tens to hundreds or more).
4) Increasing frequency of operation (to 100 GHz or higher) [11].
5) Increasingly complex multifunctional chips, for example, complete radar T/R modules on a single chip [12].
6) Increasingly affordable MMIC chips as process and design technologies mature, as yields improve, and as volumes increase, driven by emerging commercial applications such as wireless and cellular.

These trends are influencing packages and package development in a number of ways which include:

1) As operating frequencies increase, parasitics and parasitic variability resulting from mechanical tolerances and assembly techniques become increasingly important.
2) For economic and other reasons, the number of electronic functions per-package is increasing resulting in greater emphasis on RF multichip modules.
3) Multifunction RF packages require greater numbers of dc, RF, and control signal paths (I/Os).
4) Both military and commercial applications are actively working to drive down the cost of the package function.

C. New Package Material and Process Technologies

When considering the selection of a host material for monolithic microwave and millimeter-wave circuits, the fol-
allowing properties must be considered: dielectric constant, density, dissipation factor, thermal conductivity, dielectric strength, bulk conductivity, surface finish, thermal expansion coefficient, flexure strength, flatness, ease of manufacture, tolerances, ease of electrical feedthrough, and cost.

The materials may be divided into those for substrates and those for packaging. The trend is an ever-increasing interconnect density for portable and lighter weight electronics. Increased power density has stimulated the development of multilayer substrate and package materials with high thermal conductivity. The substrate is becoming an integral part of the packaging. Materials without high thermal conductivity must rely on a mechanical solution such as metallic via arrays or cutouts to reduce the thermal resistance. The laminate also has high dielectric constant and those for packaging. The trend is an ever-increasing interconnect density for portable and lighter weight electronics.

Multilayer aluminum nitride (AlN) can be manufactured at high temperatures (1900°C) with a pressure-based or pressureless process. Accurate XY registration for the pressureless process is under development at both Coors and IBM. The pressure process reduces the shrinkage in the X-Y plane to approximately 1% and 50% in the Z direction. This is a great advantage for three-dimensional (3-D) packaging since XY registration of vertical interconnects can easily be achieved for microwave interconnections. Three-dimensional packaging is the vertical interconnection of several substrates which usually increases the package density by a factor of five to six. It is presently being developed for frequencies up to 18 GHz.

Several metal matrix materials with high thermal conductivity have been developed to provide thermal expansion match to GaAs microwave devices. These materials include tungsten/copper (WCu), molybdenum/copper (Mo/Cu), and silicon carbide/aluminum (SiC/Al). The tungsten and molybdenum are mixed with about 15% copper to obtain thermal expansion coefficients slightly higher than GaAs. This places the GaAs chip under compressive stress after die attach to the metal matrix. Both materials have a thermal conductivity close to 165 W/mK at room temperature. Net shape packages have been molded from SiC/Al with tolerances approaching one part in a thousand. The thermal conductivity of this material is approximately 160 W/mK with an expansion coefficient of seven parts per million at room temperature. Kovar, which is an iron-nickel-cobalt alloy, and other iron-nickel compounds are used for packaging because they can be easily seam sealed. Their disadvantage compared to the above mentioned metal matrix materials is their poor thermal conductivity.

Table II summarizes the important advantages and disadvantages of AlN and SiC/Al, two new packaging materials which are receiving widespread attention.

D. Flip-Chip—An Alternate Low Defect Assembly Technique

Assembly processes associated with conventional face-up MMIC chips: i) contribute to a major source of yield loss to high value product, ii) are a source of parasitic variability, iii) are a major source of visual and other defects associated with die attach and wirebonding, and iv) very likely play an adverse role in reliability. For these reasons, the flip-chip mounting of MMIC and other RF devices is an attractive alternative to the conventional face-up mounting of chips.

Fig. 3 schematically depicts the two approaches. Connections between the flip-chip and substrate are made with electroformed silver bumps batch fabricated at the wafer level. The flip-chip circuit topology is uniplanar and has no backside ground plane, unlike microstrip circuits. Consequently, no backside processing (wafer thinning, via holes, or backside metallization) is required, thus reducing chip processing cost. Recently, thermal simulations have shown flip-chip circuits to have lower thermal resistance than comparable microstrip-based circuits [13].

Flip-chip MMIC devices offer additional advantages in the fabrication of high level assemblies. No wire bonding is required, and batch die bonding of multiple chip assemblies may be carried out using the surface tension of molten solder to affect precise chip/substrate alignment. The precision resulting from a carefully controlled flip-chip die attach process is sufficient for aligning chips to fibers in optical assemblies [14]. Because of this high precision, flip-chip assembly is also attractive for millimeter-wave components.

Hughes has demonstrated that flip-chip mounting has no adverse effects on the performance of MMIC chips at X-band. Repair of the process is performed commercially by directing hot air on the chip until the chip separates from the substrate. Size limitations of the MMIC chips depend on the CTE mismatch between the substrate and the GaAs, the bump height and material, and the number of required thermal cycles. Hughes has flip-chip mounted GaAs chips with dimensions of 0.181 \times 0.143 \text{ in} on AlN substrates. The bumps were 4 mils in height and composed of pure silver. The bumps were attached with lead indium solder and survived 2000 thermal cycles from −55 to 125 degrees C with no microwave performance degradation. In our experience, a MMIC die with 10 to 15 I/Os will attach with a probability better than 0.999. For example, 16 chips on a substrate will have an attachment yield of 0.98.

E. Design Tool Limitations

The limitations of the tools available to the engineer for analysis and design of microwave and millimeter-wave modules have become pronounced as the performance, packaging, and manufacturing requirements have increased. Previously, microwave modules were of low packaging density that were individually hand tuned to meet specifications. By following relatively simple design guidelines, it was possible to design and manufacture these modules. Most of the analysis was at the schematic level. Today, however, the designer is faced with higher density modules, MMIC's, new manufacturing technology, highly integrated dc (logic, control) and RF circuitry, and the requirement for module designs which require no tuning. The design engineer must be able to analyze very complex structures with many conductor and dielectric layers to determine coupling, radiation, higher order mode propagation, package resonance, MMIC interactions, and thermal performance in a real-time analysis/design environment. It is
now necessary to link the analysis to the physical layout. The ability to analyze trade-offs in material selection, functional partitioning, parts selection, and cost and manufacturability is also required. While it is possible to find commercially available software to perform a few of the above tasks, an integrated design environment does not now exist.

Although there is room for many improvements in the design tools, there are two areas where significant limitations exist. The first is electromagnetic analysis software. The design engineer would like to analyze the entire module using the EM simulator. Currently this is not possible. Most of the software currently available is based upon finite element analysis (HFSS [15], MSC/EMAS [4], Maxwell SI Eminence [16]), or the method of moments (Sonnet [17], Explorer [18], and Momentum [15]). The finite element analysis programs require large amounts of memory (256M RAM, 500M swap space) for the solution and may require excessive time (hours) to obtain a solution. Since the solution is in the frequency domain, each frequency point requires a new solution. The method of moments programs are 2.5-dimensional (2.5-D) and are not able to analyze 3-D structures. A 2.5-D simulator accounts for current in two dimensions only, although approximations for vias or other structures in the third dimension are often made. A 3-D simulator allows for currents in three dimensions. In addition, 2.5-D simulators are most often used for planar circuit analysis, such as MMIC’s, while 3-D simulation will analyze arbitrary 3-D structures. The solution times using method of moments can be significantly shorter, however, than with finite element analysis, often by an order of magnitude or more.

Table III shows currently available EM simulation tools appropriate for use in microwave package design. Shown in addition to finite element and method of moments tools are codes developed at government laboratories and universities employing finite difference time domain (FDTD) techniques. The latter are, for the most part, still being improved and not available commercially.

Currently, many designers use the software in a diaoptic or composite package mode. That is, they divide the module into subdivisions and solve each of them using the most appropriate

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**Fig. 3** (a) Comparison of face-up and flip-chip die attach techniques. (b) Silver interconnect bumps.
TABLE III
ELECTROMAGNETIC SIMULATION TOOLS FOR MICROWAVE PACKAGE DESIGN

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Analytical Methodology</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ansoft</td>
<td>Maxwell 3D Electromagnetics EM software</td>
<td>Frequency Domain</td>
<td>Similar to HFSS with additional capabilities.</td>
</tr>
<tr>
<td>Ansoft</td>
<td>Insight</td>
<td>Nonlinear 3-D frequency domain simulator</td>
<td>3-D microwave and millimeter-wave circuits.</td>
</tr>
<tr>
<td>NEC-Canada</td>
<td>HPSS</td>
<td>Finite Element Method</td>
<td>General purpose field solver.</td>
</tr>
<tr>
<td>MacNeiII</td>
<td>CS3/3SMAS</td>
<td>Frequency Domain</td>
<td>Finite element analysis of general 3-D microwave and millimeter-wave circuits.</td>
</tr>
<tr>
<td>Methods of Moments</td>
<td>software</td>
<td>Method of Moments</td>
<td>Method of Moments analysis for resonant cavities and dielectric loaded structures.</td>
</tr>
<tr>
<td>Excel (Moir)</td>
<td>XGEMS/M</td>
<td>2-D Method of Moments</td>
<td>Method of Moments analysis for planar circuits.</td>
</tr>
<tr>
<td>Compact Design</td>
<td>Momentum</td>
<td>3-D Method of Moments</td>
<td>Method of Moments analysis for planar and non-planar circuits.</td>
</tr>
<tr>
<td>NEC-Canada</td>
<td>Momentum</td>
<td>3-D Method of Moments</td>
<td>Method of Moments analysis for planar and non-planar circuits.</td>
</tr>
</tbody>
</table>

software. The resultant solutions are interconnected and the module performance is predicted. Many package effects such as resonances are lost when using this method. A desired EM analysis solution should be: i) time-domain based so that one solution can be Fourier transformed to get the frequency performance, ii) able to perform package resonance analysis, iii) have both 2.5-D and 3-D capability, and iv) have the capability to scan the layout in an automatic or manual mode, partition, and then perform the analysis.

The second major improvement needed is the integration of analysis programs with the layout environment. Currently, thermal analysis of modules in a seamless design environment is possible. Most major design environment programs offer this option. The same level of integration is needed for EM simulators and interfaces with material, interconnection, and device databases.

F. Automated Assembly and Test

Microwave production lines are being automated so that the CAD designs for the package and substrates can be directly used to develop the computer-aided manufacturing (CAM) plan. This paperless transfer of data decreases the cycle time for manufacturing and reduces errors. The key product characteristics are listed on each of the digitally encoded drawings. This allows the manufacturing engineer to set the control limits on the process parameters that can cause the key characteristics to fall outside of their specification. These processes are monitored continuously to assess their capability indexes Cpk and Ppk. Besides the normal automatic functions of pick and place, wire bonding, and flip-chip attachment, the production line is automated for test and hermetic sealing.

The flip-chip assembly process has already been proven to be a six-sigma process for silicon products by Delco Electronics in Kokomo, IN. This same technology has been applied to X-band microwave MMIC chips. From modeling with HFSS, the frequency can be extended to 50 GHz with no adverse effects on performance. Fig. 4 shows the assembly process for a flip-chip microwave package. The number of process steps has been reduced since all components including resistors and capacitors are attached using the same assembly steps. The substrate which is usually ceramic with gold metallization is printed with lead indium solder on all interconnect sites. The solder paste contains the flux required to clean the soldering surfaces. The flip-chips and other components are automatically picked and placed at the appropriate sites using pattern recognition. The machine places chips at the rate of 40 per minute. Although it has the capability of placing chips with an accuracy of one half mil, the flip-chip process only requires placement accuracy of one-half the pad size. The solder reflow operation pulls the chip bumps accurately onto the pad centers.

After placement of the component parts, the substrate is placed in the solder reflow furnace. A controlled temperature profile provides first the temperature needed to activate the flux which initiates cleaning action. The profile then increases to a temperature slightly above the solder melting point causing surface tension to self-align the chip. At present, the bumps are six mils in diameter placed onto 10-mil pads which require a placement accuracy of only ±2.5 mils. A silicon nitride passivation is used around the chip pads to prevent solder shorting to the surrounding chip metallization. This process is being used by HE Microwave in Tucson, AZ to produce...
Fig. 5. Evolution of packaging for the T/R module. Thin-film single-layer substrates with aluminum metal packages and connectors have evolved to 3-D multilayer circuitry with no connectors. (a) Single-layer thin-film substrate in metal package with conventional connectors and discrete devices. (b) First thick-film single-layer substrate. (c) Multilayer thick-film LTCC substrate with low power flip-mounted chips and no connectors. (d) All flip-chip multilayered A/N substrate.

Fig. 5. (Continued) (e) Multichannel module employing 3-D stacked multilayer thick-film A/N substrates and flip-chip MMICs.

radar transmit receive modules for military and commercial applications.

The final operation for the chip attachment is the flux removal from the substrate. These four processes: solder print, flip-chip placement, solder reflow, and flux removal complete a very reliable attachment process. The process is achieving highly reproducible results for silicon, and similar results are expected for microwave and millimeter-wave applications.

Automated module test includes phase, gain, noise figure, third-order intercept, and other measurements before and after hermetic sealing of the package. The results are compared to specification tolerance windows, and the module is passed or rejected based on the comparison. The sealing is performed automatically and can be performed by laser welding or seam sealing. Seam sealing is presently preferred because of its greater yield. Gross and fine leak testing using helium or radioactive gases is a slow process and will be replaced in the future by measuring lid deformation with a laser.

Burn-in is performed at the end of production and is initially performed on 100% of the modules. As the product matures, the burn-in percentage is reduced by lot testing. The cycle time for module assembly, test, and rework is presently being reduced by the use of solderless interconnects. These connections require pressure to make electrical contact and can be used to about 20 GHz and include fuzz buttons manufactured
Microwave products usually have a manufacturing cost of at least hundreds of dollars, so that defective modules are often repaired. The repair consists of analysis time to determine the defect and repair time to fix or replace. These operations are not automatic and can significantly affect the cycle time of manufacturing and the capacity of the test station. Also, repair may cause other visible and undetected collateral damage requiring either more repair or contributing to shorter product life. Repair of defects can significantly add to the overall manufacturing cost [19]. To reduce the cost of repair, more effort must be invested in determining and eliminating the cause(s) of the defect.

IV. T/R MODULES FOR ACTIVE ARRAY RADI—A CASE STUDY

The evolution of the T/R module for X-band active phased arrays demonstrates the revolution that has occurred in microwave packaging during the last decade and is illustrated in Fig. 5. Fig. 5(a) shows a T/R module that was manufactured in the early nineteen eighties. The modules are thin-film printed on a single layer of alumina. All of the microwave devices are discrete. The package is aluminum with conventional coaxial connectors. A major improvement was the replacement of thin-film sputtered metal with lower cost thick-film metal for printing microwave circuitry. Fig. 5(b) displays a thick-film printed circuit with a few MMIC power amplifiers. With the advent of low temperature fired ceramic technology (LTCC), multilayer microwave circuits became possible. The microwave circuits can be printed with thick-film gold, silver, or copper. Fig. 5(c) shows an example of this technology with a conventional aluminum package.

The next evolutionary improvement was the development of flip-chip assembly for microwave MMIC devices. LTCC presented a thermal barrier for high power flip-chips, and a new, more conductive material was needed for high power amplifiers in the T/R modules. Aluminum Nitride (A/N), developed in the early nineteen nineties, provides an alternative to beryllia and also allows cofiring of the substrate layers. Fig. 5(d) illustrates a multilayer A/N substrate with four transmit only circuits. All the MMIC chips are flip mounted and the internal metal layers are thick-film tungsten, while the top layer is electroless gold.

The next evolution was the achievement of very high-density microwave packaging through the construction of 3-D packaging using stacking multilayer A/N substrates. Fig. 5(e) shows a representation of this circuit which is presently in development. All of the conventional microwave I/O conductors are eliminated. The package contains multiple T/R channels in a volume much smaller than a previous single channel package. The 3-D package can be attached to the array by screws or a pressure plate. The electrical attachments can be made by solderless interconnects such as fuzz buttons or elastomerics.

This approach to packaging provides the opportunity for batch assembly and testing of T/R modules. Large substrate cards containing a single level for many modules can be populated with active and passive components which are die attached using solder reflow techniques. The individual cards are then probe tested in a manner similar to that used for semiconductor wafer level RF probing. Following 3-D stacking assembly, the modules may again be batch tested using RF probes. This approach eliminates assembly, handling, and testing of individual modules and is expected to substantially reduce module cost.

V. CONCLUSIONS AND PROGNOSIS

From the T/R module examples presented above, it is possible to summarize the thrusts of current RF package development activities as follows: a continuing drive to lower cost, increased emphasis on higher levels of package integration, more accurate and comprehensive package design and simulation tools, greater use of batch fabrication and testing, and more automated and simpler assembly processes (fewer wire bonds).

In the longer term, these trends should lead to [20]:
1) Integrated seamless package design encompassing the electrical, mechanical, and thermal environment of the active devices contained.
2) Standardized material process and test databases supporting multidimensional predictive modeling for computer aided package engineering and manufacturing.
3) Further increase in the level of package functional integration.
4) Automated intelligent semiconductor die pick, attach, tune, and test procedures to minimize and accommodate the effects of semiconductor device parameter variation.

REFERENCES


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He worked for Hughes Space and Communications group for approximately 17 years designing equipment for ranging satellites and telephone transmission and reception equipment for satellites. He was subsequently employed by Ford Western Development laboratories as the Engineering Manager for the development of satellite terminals for data transmission. He returned to Hughes Aircraft and has spent the last 10 years in the development of transmit/receive modules for active arrays. He is presently the Program Manager for Advanced Microwave Packaging Programs for the Radar and Communications group at Hughes. He hold three patents for microwave packaging and has published five journal or conference papers in the last three years regarding packaging.

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