

White Paper

Analog Versus Digital Beam Forming



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Introduction

Active Electronically Scanned Array (AESA) radar has been proposed for many Department of Defense (DoD). While an AESA is likely the best solution, there is another level of options for the AESA. This is because they can be realized using analog beam steering or

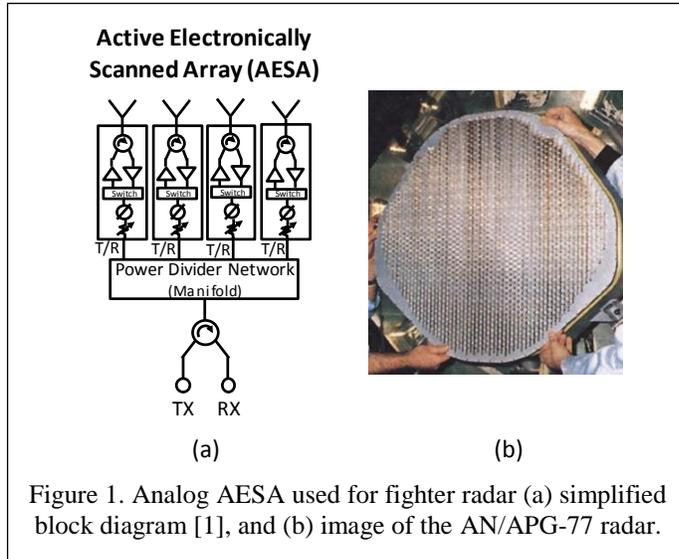


Figure 1. Analog AESA used for fighter radar (a) simplified block diagram [1], and (b) image of the AN/APG-77 radar.

digital beam steering. Figure 1(a) illustrates a simplified block diagram of an AESA using analog beam steering. It uses individual transmit/receive modules with phase shifter to achieve beam steering. This type of radar is state of the art for radars that are deployed on numerous platforms. Figure 1(b) shows the AN/APG-77 radar which is an analog AESA.

The benefits of this type of radar are significant since it has no moving parts. This means that it is much more reliable than prior generations of radars that used mechanical steering to for

search and tracking of targets. Also, this type of radar allows for tracking of several targets by using complex beam forming methods. However, a significant disadvantage is that it has a limit on the number of target that it can simultaneously track.

Digital Beam Forming

One method to improve the ability of an AESA to track multiple simultaneous targets is to use digital beam forming. Digital beam forming uses circuitry that is a departure from the normal T/R module. Instead of using phase shifters at each element in the phased array, the radar beam is steered digitally since the digital functions are pushed forward into the system. The digital sampling occurs at the antenna element on both transmit and receive.

In the simplest case, the digital beam forming T/R module consists of front filtering, low noise amplifier, high power amplifier, and mixing along with analog to digital conversion. In a practical system, the block diagram will be more complicated. For instance, the LNA and HPA will likely be multistage and there may be additional filters and other components in the system. A simplified block diagram of one element in a digital beam forming array is shown in Figure 2. Note that this block diagram is repeated for each element in the array.

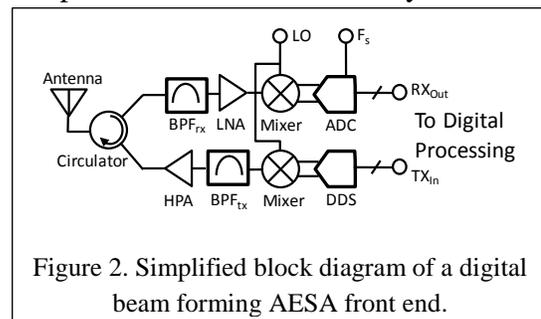


Figure 2. Simplified block diagram of a digital beam forming AESA front end.

Challenges with Digital Beam Forming

There are several challenges with using digital beam forming. The first is the amount of data that is generated. Considering the receive portion of the digital receiver, one of the most important points to consider the data rate out of the ADC. This is important since it impacts the digital interface requirements and processing power requirements of the digital portion. The data rate at the point RXout is given by

$$\text{Data Rate at RXout} = F_s \cdot N + \text{Control Bits} + \text{Status Bits} \quad (10.1)$$

Where:

F_s = sample rate of the ADC (MSPS)

N = number of bits in the ADC

ADC = analog to digital converter

Control Bits = the data rate of the control bits that control the function of the ADC

Status Bits = the data rate of the status bits out of the ADC such as the over range bit

In most applications the data rate of Control Bits and Status Bits will be much lower than the Data Rate at RXout and so we will neglect their contribution to the overall data bandwidth. Consider an example where the ADC has 16 bits and a sample rate of 100 MSPS. In this case, the Data Rate at RXout will be equal to $100 \times 16 = 1.6\text{GSPS}$ per element in the array. This means that for an 8×8 array, the total data rate out of the RXout ports will be $1.6\text{GSPS/element} \times 64\text{ elements} = 102.4\text{GSPS}$. This illustrates one of the important design considerations for digital beam forming which is the handling of the data. While it is true that some systems can achieve performance with few bits in the ADC, and some systems do not need to sample at 100 MSPS, the trend in radar systems is more bits for increased resolution and higher sampling rate for increased bandwidth.

Another concern about digital beam forming is the power consumption required by the processing. While it is possible to procure ADCs with reasonable power dissipation, the FPGA and other processors require significant power. The FPGA and processors perform the important function of combining the signals from multiple elements, processing of the signals, and data packaging for transport to the next level in the system (additional processing and signal analysis). Because of the limitation in data bandwidth, there is a practical limit on the number of elements (channels) in the array that a FPGA can handle. For instance, if a FPGA is used to capture data from four elements in an array with 16 bit ADCs running at 100MSPS, then the data rate out of the FPGA will be $1.6\text{GSPS} \times 4 = 6.4\text{GSPS}$. While the FPGA may be able to handling pumping out that data rate, the digital interface to the next level becomes a concern even if high speed interfaces are used.

Conclusions

Despite the data handling concerns, the possibility of tracking multiple targets makes the digital beam forming approach very attractive for some applications. This is especially true for military systems which must track an increasing number of targets.

On transmit, a fully digital beam formed array requires the use of waveform generators at each of the elements. This can create complications in the design of the array, though some have attempted to achieve this using direct digital synthesis of the waveforms at each element and then using a frequency mixer to up convert the waveform to the desired transmit frequency.

References

[1] Used with permission from: R.L. Sturdivant, Mike Harris, *Transmit Receive Modules for Radar and Communication Systems* (Norwood, MA: Artech House, 2015).